URN etd-0407109-183725-2107
Author Pai-Fu Hung
Author's Email Address No Public.
Statistics This thesis had been viewed 63 times. Download 35 times.
Department
Year 2003
Semester 2
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title Antenna/CMOS Integrated Circuit for IEEE 802.11a Wireless LAN
Date of Defense 0000-00-00
Page Count 76

Keyword
5.25 GHz
IEEE 802.11a wireless LAN
0.18 μm CMOS
antenna
T/R switch
low-noise amplifier
mixer
Integrated Circuit

Abstract
This study proposes the development of the 5.25 GHz antenna and CMOS RFIC in a 0.18 μm CMOS technology for IEEE 802.11a wireless LAN. The CMOS front-end includes a transmitter/receiver switch (T/R switch), a low-noise amplifier (LNA) and a mixer. The antenna provides the advandages of the low return loss and great pattern. The T/R switch provides several advantages, such as the low insertion loss, high isolation, low voltage, lower noise and high gain. For the mixer, it exhibits the high linearity and isolation so as to boost the performance of the whole RF front-end.

The antenna exhibits a input return loss (S11) less than —10 dB, a bandwidth larger than 200 MHz, and a great omnidirectional pattern. This chip uses a standard 0.18 μm CMOS technology. The T/R switch exhibits a S11 less than —16.7 dB on transmitter or receiver port, the antenna exhibits a S11 less than —15.3 dB, an insertion loss less than 2.6 dB, an isolation of 20.6 dB, an input P1dB of 16 dBm. The LNA exhibits a S11 less than —16.1 dB, a S22 less than —25 dB, a gain larger than 24.5 dB, a noise figure less than 2.93 dB, an input P1dB of —19 dBm, and an IIP3 of —12.15 dBm. The mixer exhibits a S22 less than —32.7 dB, a conversion gain of —5.7 dB, a P1dB of —10 dBm, an IIP3 of —0.6 dBm, an isolation at LO to IF of —86.8 dB, and an isolation at RF to IF of —123.5 dB. The whole RF front end exhibits a input return loss less than —16.1 dB, a conversion gain of 17.2 dB, a noise figure of 4.85 dB, an IIP3 of —35.27 dBm. It will be integrated with the following stages in the future to meet the system-on-chip (SOC) goal.
Advisory Committee Yu-Shyan Lin - advisor

Files etd-0407109-183725-2107-001.pdf

indicate access worldwide
Date of Submission 2004-07-08